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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,879	12/28/2000	Aditya Mukherjee	42390P9572X	9416

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,879	MUKHERJEE, ADITYA	
	Examin r	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- Th MAILING DATE of this communication appears on the cov r she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/04/04* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

NON-FINAL OFFICE ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection on 4 Sept. 2004. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission jointly filed has been entered.

1.0 This office action is in response to such Applicants' Amendment/submission.

1.1 **Claims 1, 6, 11** and **16** are amended. **Claims 1-20** remain pending.

1.2 The objections and rejections of record are withdrawn in response to Applicants' amendment.

Response to Arguments

2. Applicants' arguments of 4 Sept. 2004 have been fully considered and are persuasive only to the extent that the feature whereby 'snapshot instruction and a shift instruction are partitioned into separate operations not requiring synchronization' is not specifically described in detail by the prior art of record.

Said feature is supported by newly found reference, e.g., in Fig. 7 and col. 5 line 55 et seq. (initial/shift/snapshot modes), of **Borden** (US Patent No. 5,790, 561; 4 Aug. 1998), as follows.

Claim Rejections - 35 USC ' 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

3.1 **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wasson** (US Patent No. 6,181,151; filed 28 Oct. 1998) in view of **Attaway et al.** (US Patent No. 5,701,308; 23 Dec. 1997) in further view of **Borden et al.** (US Patent No. 5,790, 561; 4 Aug. 1998).

As per Claims 1, 6, 11, 16, Wasson substantially depicts, in Figs. 1-2 and related description in col. 1 line 10 et seq., the claimed apparatus or system or means circuit comprising: internal data bus (col. 2 line 55, or Fig. 1 numeral 24); plural clusters coupled to said bus with data signal synchronizing means for data signals there-through (Fig. 1 CH1..CHN);

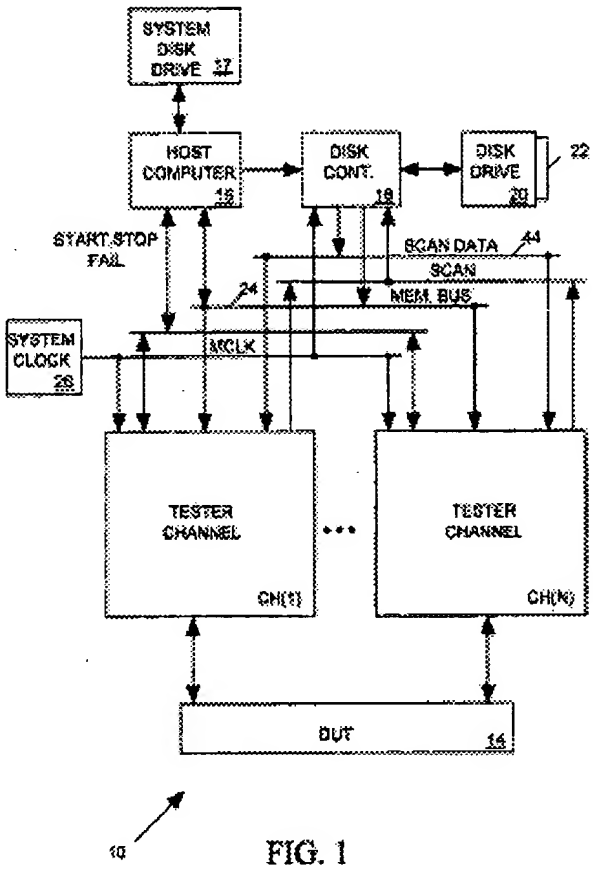

FIG. 1

test controller coupled to said bus (col. 4 line 45 or col. 6 line 50 et seq., as seen in Fig. 1 Blocks 16 and 18); and a debug or tester or tester unit coupled to said bus (col. 4 line 47 et seq.) wherein the bus is configured to generate system or global control signal (at col. 4 lines 46 et seq.) and each of said plural clusters configured to generate local or separate control signals at col. 4 lines

49 et seq., wherein an IC embeds said ITC, clock controller means and entire tester components within a monolithic integrated circuit, e.g., in Fig. 1 and col. 3 line 45.

Not specifically described in detail by **Wasson** is the step whereby the ITC has an instruction register and a test access port finite state machine and the tester is embedded along with the device under test in an IC.

However, Examiner notes that such **ITC** comprising an instruction register and a test access port finite state machine is part of a design standard as described in IEEE 1149.1, as conceded by Applicants' instant application on page 9 line 4. **Examiner** also notes that **Wasson** teaches the use of a finite state machine in Fig. 2 and memory means to store test instructions in plural channels in, e.g., col. 7 line 4.

Accordingly, such ITC so configured is well known as being part of an integrated circuit, said IC having a self-test feature. It is also is well known that some ICs comprise built-in self-testing (BIST) capabilities thereby **obviating the need for a bulky/expensive external tester and costly maintenance associated therewith**. For instance, **Attaway et al.** incorporates such design approach for a BIST system as depicted in Fig. 4 wherein *interface 10* comprises a *finite state machine 50* and *an instruction register 52*. {See **Attaway et al.**, Id., e.g., col. 3 line 25 for IEEE 1149.1 standard, col. 5 lines 34 for TAP finite state machine, col. 4 line 39 for instruction register, and RAM and *RAM BIST 40.*}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the IC tester of **Wasson** by including therein TAP state machine and instruction register with a BIST system as taught by **Attaway et al.,** because such modification would provide the testing procedure of **Wasson** with a method whereby the testing system not only complies with the IEEE 1149.1 standard but also is cost efficient because such

design minimizes test hardware overhead and eliminates operator intervention in test mode. {See **Attaway et al,** Id., Fig. 4: block 10.}

While Wasson and **Attaway** substantially disclose the procedure for the claimed method or apparatus, they **fail to specifically mention** that the snapshot instruction and shift instruction are partitioned into separate operations not requiring synchronization.

However Borden, in an analogous art, discloses internal testability system for microprocessor IC depicted, e.g., in Fig. 7 (below) and related description in paras. 18 (initial mode) and 24 et seq. (shift mode) wherein a *local controller 140* latches global control signals, such as *shift, compress and snapshot, separately synchronized,* in response to local timing to generate local control signals based on the phase of local clocks to collectively control plural MISRs.

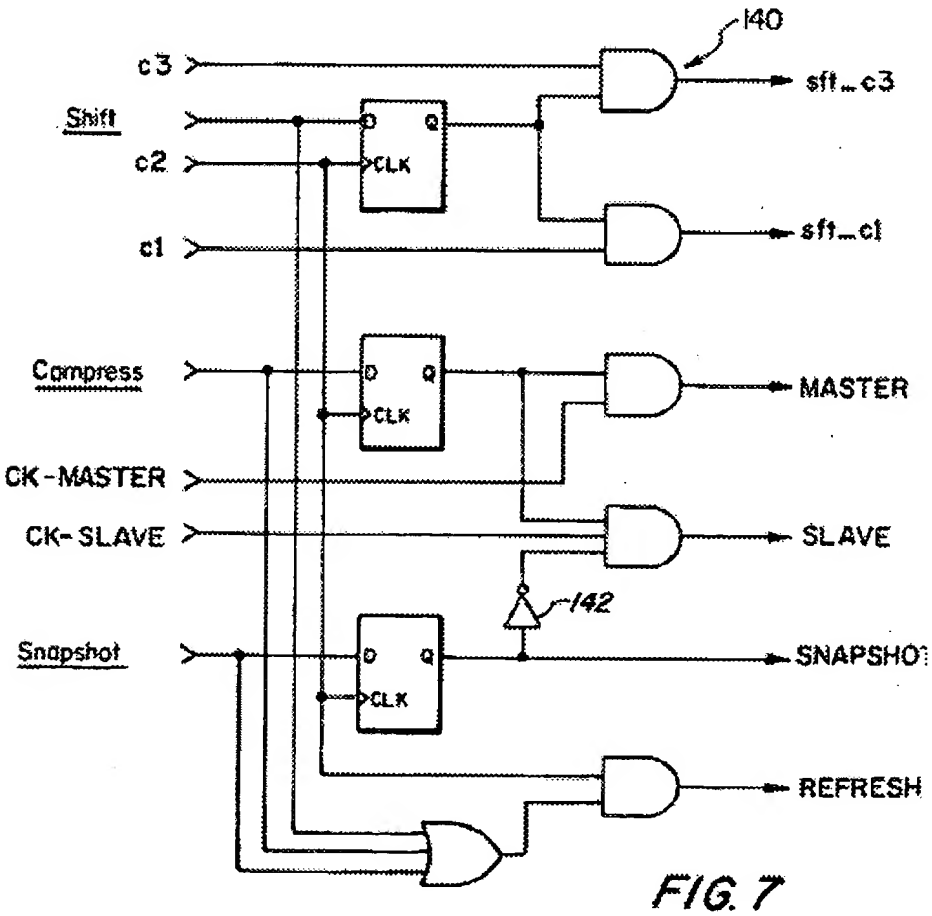

FIG. 7

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Wasson** and **Attaway** by including therein a snapshot/shift timing technique as taught by **Borden,** because such modification would provide the procedure disclosed in **Wasson** and **Attaway** with a technique whereby "snapshot and shift global signals can be combined to rapidly initialize all MISRs ***at initialization, e.g., "In*** *particular, the snapshot signal (FIG. 6 to FIG. 7) generates a local signal snapshot which turns on a transistor 226 (FIG. 7 to FIG. 8) that forces the output of the slave latch 220 to one. The shift signal (FIG. 6 to FIG. 7) causes a subsequent shift clocking sft.sub.-- c3, sft.sub.-- c1 (FIG. 7 to FIG. 8) that feeds the one from each slave 220 into the master 210 of the next stage through a transistor 216, causing the master 210 to latch a zero."* {See **Borden et al.,** col. 5 line 62 et seq.}

As per Claims 2, 17, Wasson depicts, in Fig. 2 and related description in col. 4 line 55 et seq., the claimed timing or sync or deskew buffer or memory means (Fig. 2 timing circuit 36) along with local clock driving means effected by Fig. 2 formatting circuit 38 as described in col. 5 line 27 et seq.

As per Claims 3, 7, 12, 18, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent test control distribution means.

As per Claims 4, 8, 13, 19, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent snapshot instruction and shift instruction means, e.g., in Fig. 2 block 46 and col. 6 line 2-3, 43 et seq.

As per Claims 5, 9, 14, 20, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent snapshot instruction and shift instruction means, e.g., in Fig. 2 block 46 and col. 6 line 2-3, 43 et seq.

As per Claim 10, 15, Wasson depicts, in Fig. 2 and related description in col. 6 line 62 et seq., the claimed debug or test triggering means via variable time period under control of state machine 34 of Fig. 2.

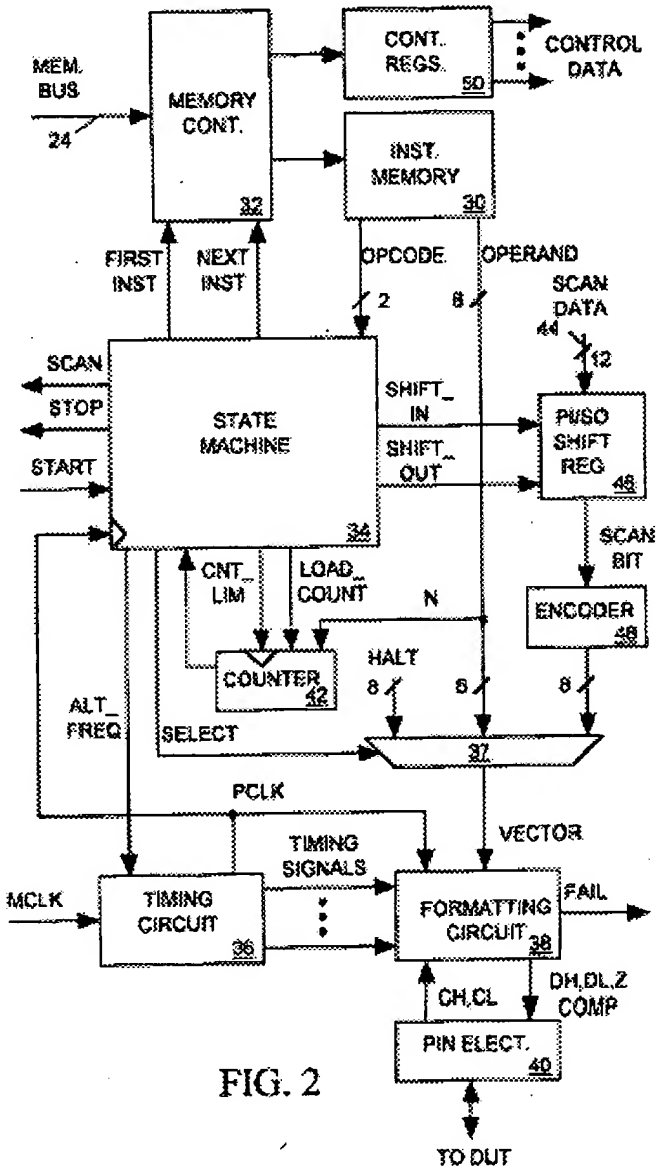

FIG. 2

Conclusion

4. Any response to this action should be mailed to:

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or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
1/3/05